47. (Amended) [A] The memory [cell] device according to claim 26, wherein the second plate also surrounds first plates of adjacent memory cells.

48. (Amended) [A] The memory cell according to claim 31, wherein the second plate also surrounds first plates of adjacent memory cells.

49. (Amended) [A] The memory cell according to claim 33, wherein the second plate also surrounds first plates of adjacent memory cells.

50. (Amended) [A] The memory [cell] device according to claim 35, wherein the second plate also surrounds first plates of adjacent memory cells.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on October 29, 2002, and the references cited therewith.

Claims 26, 31, 35, 36, 40, 41, 43-50 are amended, claim 51 is canceled; as a result, claims 17-19, 22, 23, 25-27, 29, and 31-50 are now pending in this application.

Information Disclosure Statement

Applicant respectfully requests that a copy of the 1449 Form, listing the references under "other documents" section, that were submitted with the Information Disclosure Statement filed on December 20. 1999, marked as being considered and initialed by the Examiner, be returned with the next official communication.

Copies of the references under the "other documents" section were submitted in the parent application. However, Applicant has included copies of these references again in this amendment and response.

§112 Rejection of the Claims

Claim 43 was rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claim 43 depends on claim 41. Applicant has amended claim 41 to remove the term "lateral". Thus, claim 43 is now consistent with claim 41. Applicant requests that the rejection be withdrawn.

§103 Rejection of the Claims

Claims 17-19, 31-33, 37-38, 41-46, 48-49, and 51 were rejected under 35 USC § 103(a) as being unpatentable over Pfiester (U.S. 4,761,385) in view of Kanetaki et al. (U.S. 4,906,590).

Independent claims 17, 31, 33, and 41 recite a transistor having source/drain regions formed "outwardly" form a substrate. Pfiester discloses a different kind of transistor. Pfiester discloses a transistor having source/drain regions formed *within* a substrate. Thus, Pfiester does not disclose a transistor having source/drain regions formed "outwardly" form a substrate. Kanetaki et al. also does not disclose a transistor having source/drain regions formed "outwardly" form a substrate. Since Pfiester and Kanetaki et al. do not disclose all features recited in claims 17, 31, 33, and 41, these claims and their dependent claims are patentable over Pfiester and Kanetaki et al. Therefore, Applicant requests that the rejection be reconsidered and withdrawn and that claims 17-19, 31-33, 37-38, 41-46, and 48-49 be allowed.

Claims 22-23, 25, 34, and 39 were rejected under 35 USC § 103(a) as being unpatentable over Itoh '389 in view of Kanetaki et al. (U.S. 4,906,590).

Independent claims 22 and 34 recite a memory cell having a "vertical transistor" and a source/drain region, in which the source/drain region includes integral therewith a first plate having a polycrystalline surface layer with "etch-roughened" surface.

Itoh does not disclose a memory cell having the "etch-roughened" surface feature. Kanetaki et al. do not disclose a "vertical transistor". Neither Itoh nor Kanetaki et al. suggests any reason for combining these two features.

Itoh discloses a memory cell array having structure adapted "to attain a high scale of integration". Itoh has no motivation to have a polycrystalline surface layer with "etch-roughened" surface. Itoh explicitly states the high scale of integration purpose in column 3, lines 35-39. Kanetaki et al. has no mention at all about "vertical transistor". Since Itoh has no teaching, suggestion, or motivation to have a polycrystalline surface layer with "etch-roughened" surface, and Kanetaki et al. has no teaching, suggestion, or motivation to have a "vertical transistor", there is no reason to combine the Itoh and Kanetaki et al. references to achieve a combination of a "vertical transistor" and a polycrystalline surface layer with "etch-roughened" surface as claimed in claims 22 and 34 of the present invention.

Further, the fact that references may be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP § 2143.01. Itoh has no teaching, suggestion, or motivation to have a polycrystalline surface layer with "etch-roughened" surface. Kanetaki et al. has no mention at all about "vertical transistor". Thus, the combination of the Itoh and Kanetaki et al. references not render the *combination* of a "vertical transistor" and a polycrystalline surface layer with "etch-roughened" surface obvious.

Moreover, the teaching or suggestion to make the claimed combination must both be found in the prior art, not in Applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. Hindsight must be avoid. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). Neither Itoh nor Kanetaki et al. teaches or suggests the claimed *combination* in the claims of the present invention. Thus, the obviousness rejection is based on Applicant's disclosure.

Based on all of the reasons represented above, claims 22 and 34 and their dependent claims are patentable. Accordingly, Applicant requests that the rejection be reconsidered and withdrawn and that claims 22-23, 25, 34, and 39 be allowed.

Claims 26-27, 29, 35, 36, 40, 47, and 50 were rejected under 35 USC § 103(a) as being unpatentable over Pfiester (U.S. 4,761,385) in view of Kanetaki et al. (U.S. 4,906,590) as applied to claims 17-9, 31-33, 37-38, 41-46, 48-49, and 51 above, and further in view of Wahlstrom 5,396,452.

Independent claims 26 and 35 are amended to define that the access transistor is a "vertical" access transistor. None of Pfiester, Kanetaki et al., and Wahlstrom discloses a "vertical" access transistor. Thus, claims 26 and 35 and their dependent claims are patentable. Accordingly, Applicant requests that the rejection be reconsidered and withdrawn and that claims 26-27, 29, 35, 36, 40, 47, and 50 be allowed.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative, Viet Tong at 612-373-6969 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6969

Date 1-29-03 By _____

Viet V. Tong
Reg. No. 45,416

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 29th day of January 2003.

Amy Moriarty _____
Name Signature